North Holland
Microprocessing and Microprogramming 20 (1987) 353–354

Subject Index to Volume 20

Asynchronism 20 (1987) 287

BOSS 20 (1987) 161

CAD Tools 20 (1987) 179
CMOS 20 (1987) 153
Communications Q-Bus Interface 20 (1987) 55
Computation Problem 20 (1987) 107
Computer Hardware Description Languages 20 (1987) 161
Control Flow Checking 20 (1987) 249
Control Tasks 20 (1987) 65
Controllability 20 (1987) 287
Convolution 20 (1987) 133
Coverage 20 (1987) 309
CSMA/CD Network 20 (1987) 69

Data Driven Machine 20 (1987) 99
Datagram Service 20 (1987) 59
DEC VAX Systems 20 (1987) 73
Delay Minimization 20 (1987) 127
Design Automation Language 20 (1987) 173
Diagnosability 20 (1987) 323
Discrete Fourier Transform 20 (1987) 133
Distributed Control 20 (1987) 69
Distributed Systems 20 (1987) 39
Duplication 20 (1987) 271
Dynamic Vertical Migration 20 (1987) 197

Error Correcting Code 20 (1987) 15
Error Coverage 20 (1987) 331
Error Detection Codes 20 (1987) 331
Error Detection Technique 20 (1987) 3
Ethernet Protocols 20 (1987) 73
Exception Handling 20 (1987) 85

Fail-Soft Degradation 20 (1987) 11
Fault Detection 20 (1987) 249
Fault Diagnosis 20 (1987) 39, 301, 323
Fault Model Concurrent Test 20 (1987) 309
Fault Tolerance 20 (1987) 11, 113, 271, 287, 301, 323
Fault Tolerant CPU 20 (1987) 3
Fault Tolerant Programs 20 (1987) 33
Fault-Tolerant Distributed Computer Systems 20 (1987) 25
Fault-Tolerant Multiplier 20 (1987) 15
Fault-Tolerant Networks 20 (1987) 331
File Transfer Capability 20 (1987) 73
Finite State Machines 20 (1987) 179
Functional Language Directed Machine 20 (1987) 99

Gallium Arsenide (GaAs) 20 (1987) 121
Gate Arrays 20 (1987) 287
General Heap Processor 20 (1987) 217

Hardware Description Language 20 (1987) 183
Hierarchical Graph Model 20 (1987) 183
High Integrity Systems 20 (1987) 287

Instruction Set Design Considerations 20 (1987) 99
Instruction-Set Based Data Processing Devices 20 (1987) 147
Inter-Processor Communications Delay 20 (1987) 113
Interconnection Memory Management Unit 20 (1987) 197
Interrupt Service Routines 20 (1987) 85
ISO/OSI Session Layer 20 (1987) 59
Iterative Systems 20 (1987) 141

Kernel 20 (1987) 91

Layout Topology 20 (1987) 189
Linear Feedback Shift Register 20 (1987) 309
Local Detectability 20 (1987) 147
Logic Array Structures 20 (1987) 173
Loop Control 20 (1987) 203

Memory Management 20 (1987) 217
Message Handling 20 (1987) 59
Microprocessor-Based LAN 20 (1987) 59
Microprogrammed Control Unit 20 (1987) 309
Microprogram Control Units 20 (1987) 271
Microprogram Rollback 20 (1987) 3
Mission Time Improvement 20 (1987) 287
MML Language 20 (1987) 91
Modelling 20 (1987) 323
Multi-Microprocessor Architecture 20 (1987) 113
Multiple Processor Systems 20 (1987) 249
Multiprocessor 20 (1987) 301
Multiprocessor Real-Time Systems 20 (1987) 85

N-Adjacent Code 20 (1987) 271

Observability 20 (1987) 287
On-Line Monitoring 20 (1987) 249

Operating System 20 (1987) 301
Operating System Service Routines 20 (1987) 85

Parallel Processor 20 (1987) 107
Parallel Test 20 (1987) 283
Parametrization 20 (1987) 179
Partial Differential Equations 20 (1987) 113
Partitioning 20 (1987) 287
Personal Computers 20 (1987) 73
Physical Redundancy 20 (1987) 15
PLA Control Structures 20 (1987) 179
PLA Implementation 20 (1987) 173
Polynomials 20 (1987) 107
Process Synthesis 20 (1987) 25

Random Errors 20 (1987) 331
Reconfiguration 20 (1987) 331
Reconfiguration Algorithm 20 (1987) 127
Reconfiguration Phases 20 (1987) 11
Recovery 20 (1987) 331
Redundancy 20 (1987) 331
Reliability Hardware 20 (1987) 235
Replacement Algorithms 20 (1987) 197
Resident Software 20 (1987) 55
Residue Number System 20 (1987) 15
Retry 20 (1987) 331
RISC 20 (1987) 99
RISC Architecture 20 (1987) 223
Roving Monitoring 20 (1987) 249

Scheduling Algorithm 20 (1987) 283
Scheduling Method 20 (1987) 107
Serial Signal Processing 20 (1987) 133
Signature Analysis 20 (1987) 309
Silicon Compiler Preprocessor 20 (1987) 167
Single-Chip Microprocessor 20 (1987) 69
SPH-Graph 20 (1987) 183
System Diagnosis 20 (1987) 283
System-Level Diagnosis 20 (1987) 323
Systolic Arrays 20 (1987) 121, 133

Tagged Architecture 20 (1987) 99
Test Graph 20 (1987) 283
Testing 20 (1987) 323
Testing and Diagnosis 20 (1987) 235
Tightly Coupled Multiprocessor Systems 20 (1987) 11
TMR 20 (1987) 287
Totally Self-Checking Checkers 20 (1987) 271
TP Microcomputers 20 (1987) 227
Transaction Processing 20 (1987) 79
Transient Faults 20 (1987) 3
Two-Rail Code 20 (1987) 271

Unidirectional Errors 20 (1987) 331
UNIX Microcomputer 20 (1987) 47
UNIX Multiprocessor System 20 (1987) 79
User Interface 20 (1987) 73

Virtual Machine 20 (1987) 209
VLSI 32-Bit Microprocessor 20 (1987) 223
VLSI Designs 20 (1987) 179
VLSI-Heuristics 20 (1987) 189
VLSI-Multiplier 20 (1987) 153
VLSI/WSI Array Processors 20 (1987) 127
VMEbus 20 (1987) 65

Wide Area Network 20 (1987) 47
WSI Implementation 20 (1987) 121

X.25 Protocol 20 (1987) 55

North Holland
Microprocessing and Microprogramming 20 (1987) 355–357

Author Index to Volume 20

Adam, P., *see* Przemyslaw, B. 20 (1987) 167
Albert, M., *see* Mahler, H. 20 (1987) 179
Ancona, M., Clematis, A., De Floriani, L. and Puppo, E., A Hardware Description Language Based on a Hierarchical Graph Model 20 (1987) 183
Ancona, M., Clematis, A., Dodero, G., Fernandez, E.B. and Gianuzzi, V., Using Different Language Levels for Implementing Fault Tolerant Programs 20 (1987) 33
Andriessen, J.H.M., Polynomials on the Delft Parallel Processor 20 (1987) 107
Antola, A., Breveglieri, L. and Scarabottolo, N., Designing and Testing of a Microprogrammed Fault Tolerant CPU 20 (1987) 3
Azaria, H. and Veler, Y., Machine Instructions of a Data-Driven Architecture – Design Considerations 20 (1987) 99

Baitinger, *see* Mahler, H. 20 (1987) 179
Becker, B. and Soukop, H., CMOS Stuck-Open Self-Test for an Optimal-Time VLSI-Multiplier 20 (1987) 153
Bernandez, J., *see* Mandado, E. 20 (1987) 203
Berzieri, M., *see* Piuri, V. 20 (1987) 15
Bisaschi, A., *see* Piuri, V. 20 (1987) 15
Brause, R., *see* Dal Cin, M. 20 (1987) 301
Breveglieri, L., *see* Antola, A. 20 (1987) 3
Bruschi, O., Negrini, R. and Ravaglia, S., Systolic Arrays for Serial Signal Processing 20 (1987) 133
Burd, N.C., The Development and Performance of a CSMA/CD Network for Low Level Distributed Control 20 (1987) 69
Buschke, R., *see* Grass, W. 20 (1987) 161

Cajani, V., Architectural Issues in Designing a Unix Multiprocessor System 20 (1987) 79
Chao, Y., Jia Dong, X. and Ting, G.W., The TP Microcomputer in China: How Little Workhorses from a Small Laboratory Become Widely Used in a Huge Country 20 (1987) 227
Chernykh, E.V., Efimov, L.G., Kolpakov, I.F. and Smirnov, V.A., VMEbus in Relativistic Nuclei Research and Control Tasks 20 (1987) 65
Ciminiera, L., Demartini, C., Nicola, E., Samarotto, R. and Valenzano, A., Design and Implementation of an ISO/OSI Session Layer for a Microprocessor-Based LAN 20 (1987) 59
Clematis, A., *see* Ancona, M. 20 (1987) 33
Clematis, A., *see* Ancona, M. 20 (1987) 183
Crespi Reghizzi, S., *see* Ferrari, R. 20 (1987) 91
Curti, R., Tightly Coupled Multiprocessor Systems with High Availability Exploiting Fault-Tolerance Features 20 (1987) 11

Dal Cin, M., Brause, R., Lutz, J., Dilger, E. and Risse, Th., ATTEMPTO: An Experimental Fault-Tolerant Multiprocessor System 20 (1987) 301
Davies, O.J., *see* Osmany, J. 20 (1987) 287
De Floriani, L., *see* Ancona, M. 20 (1987) 183
Demartini, C., *see* Ciminiera, L. 20 (1987) 59
Dilger, E., *see* Dal Cin, M. 20 (1987) 301
Dodero, G., *see* Ancona, M. 20 (1987) 33
Duran, J. and Mangir, T., Application of Signature Analysis to the Concurrent Test of Microprogrammed Control Units 20 (1987) 309

Eberbach, E., *see* Just, J.R. 20 (1987) 25
Efimov, L.G., *see* Chernykh, E.V. 20 (1987) 65
Ergang, K., *see* Tellez-Giron, R. 20 (1987) 147

Fabi, A., *see* Piuri, V. 20 (1987) 15
Farina, J., *see* Mandado, E. 20 (1987) 203
Fernandes, E.S.T., *see* Vasconcelos, N.Q. 20 (1987) 209
Fernandez, E.B., *see* Ancona, M. 20 (1987) 33
Ferrari, R., Tagliabue, M., Zoccolante, L. and Crespi Reghizzi, S., Implementing the Kernel for the Concurrent Distributed Language MML on Different Microprocessors 20 (1987) 91
Franca, F.M.G., *see* Vasconcelos, N.Q. 20 (1987) 209

Gianuzzi, V., *see* Ancona, M. 20 (1987) 33
Grass, W., Buschke, R. and Rauscher, R., BOSS – A Functional Block-Oriented Intermediate Language for RT-Level Hardware Descriptions 20 (1987) 161

Hakimi, S.L., *see* Kreutzer, S.E. 20 (1987) 323
Halatsis, C., *see* Paschalis, A.M. 20 (1987) 271

Huang, K., *see* Ni, P. 20 (1987) 283
Hunger, A., *see* Tellez-Giron, R. 20 (1987) 147

Jia Dong, X., *see* Chao, Y. 20 (1987) 227
Just, J.R. and Eberbach, E., The Synthesis of Control Algorithms for Fault-Tolerant Distributed Computer Systems 20 (1987) 25

Koke, H., Integration of Personal Computers with DEC VAX Systems: Experiences With Different Ethernet Protocols in a Scientific Computation Centre 20 (1987) 73
Kolpakov, I.F., *see* Chernykh, E.V. 20 (1987) 65
Kozlowski, W.E., *see* Krawczyk, H. 20 (1987) 39
Krawczyk, H. and Kozlowski, W.E., Fault Diagnosis in Distributed Systems with Incomplete Tests 20 (1987) 39
Kreutzer, S.E. and Hakimi, S.L., System-Level Fault Diagnosis: A Survey 20 (1987) 323

Lesjak, I., *see* Trobec, R. 20 (1987) 55
Lombardi, F., Guest Editorial – Special Issue on Fault Tolerant Computing 20 (1987) 233
Luque, E., Sorribes, J. and Ripoll, A., Coprocessor for Real-Time Dynamic Vertical Migration 20 (1987) 197
Lusiani, P., DALLAS: Design Automation Language for Logic Array Structures 20 (1987) 173
Lutz, J., *see* Dal Cin, M. 20 (1987) 301

Maccianti, T., *see* Zulian, F. 20 (1987) 223
Mahler, H., Albert, M. and Baitinger, U.G., PICASSO – An Experimental CAD Tool for the Parametrization of PLA Control Structures 20 (1987) 179
Malek, M. and Yau, K.H., Cost-Effectiveness Error Detection Codes in Multicomputer Networks 20 (1987) 331
Mandado, E., Bernardez, J. and Farina, J., Hardware for Automatic Nested Loop Control in Microprogrammable Systems 20 (1987) 203
Mangir, T., *see* Duran, J. 20 (1987) 309
Menu, J., Sanchez, E., Sommer, P., HIP, A General Heap Processor 20 (1987) 217

Negrini, R., *see* Bruschi, O. 20 (1987) 133
Ni, P. and Huang, K., Parallel Testing for System Diagnosis and a Scheduling Algorithm 20 (1987) 283
Nicola, E., *see* Ciminiera, L. 20 (1987) 59
Nicolaidis, M., Evaluation of a Self-Checking Version of the MC68000 Microprocessor 20 (1987) 235

Osmany, J. and Davies, O.J., A Fault Tolerant Controller for High Integrity Systems 20 (1987) 287

Paschalis, A.M., Halatsis, C. and Philikyprou, G., Concurrently Totally Self-Checking Microprogram Control Unit with Duplication of Microprogram Sequencer 20 (1987) 271
Philikyprou, G., *see* Paschalis, G. 20 (1987) 271
Piuri, V., Berzieri, M., Bisaschi, A. and Fabi, A., Residue Arithmetic for a Fault-Tolerant Multiplier: The Choice of the Best Triple of Bases 20 (1987) 15
Przemsyslaw, B. and Adam, P., LIDO – A Silicon Compiler Preprocessor 20 (1987) 167
Puppo, E., *see* Ancona, M. 20 (1987) 183

Rajaraman, V., *see* Siva Ram Murthy, C. 20 (1987) 113
Rauscher, R., *see* Grass, W. 20 (1987) 161
Ravaglia, S., *see* Bruschi, O. 20 (1987) 133
Ripoll, A., *see* Luque, E 20 (1987) 197
Risse, Th., *see* Dal Cin, M. 20 (1987) 301
Rojatti, P. and Spalla, M., Design and Implementation of a UNIX Portable Communication Handler for a Wide Area Network 20 (1987) 47
Rubio, A., Design of Easily Testable Iterative Systems 20 (1987) 141

Samarotto, R., *see* Ciminiera, L. 20 (1987) 59
Sanchez, E., *see* Menu, J. 20 (1987) 217
Scarabottolo, N., *see* Antola, A. 20 (1987) 3
Schmitt, F.J., Module Design for VLSI-Heuristics to Optimize Layout Topology 20 (1987) 189
Schrott, G., A Generalized Task Concept for Multiprocessor Real-Time Systems 20 (1987) 85
Sciuto, D., A Reconfiguration Algorithm for Delay Minimization in VLSI/WSI Array Processors 20 (1987) 127
Shen, J.P. and Tomas, S.P., A Roving Monitoring Processor for Detection of Control Flow Errors in Multiple Processor Systems 20 (1987) 249
Siva Ram Murthy, C. and Rajaraman, V., A Multi-Microprocessor Architecture for Solving Partial Differential Equations 20 (1987) 113
Smirnov, V.A. *see* Chenrykh, E.V. 20 (1987) 65
Sommer, P., *see* Menu, J. 20 (1987) 217
Sorribes, J., *see* Luque, E. 20 (1987) 197
Soukop, H., *see* Becker, B. 20 (1987) 153
Spalla, M., *see* Rojatti, P. 20 (1987) 47
Subelj, M., *see* Trobec, R. 20 (1987) 55

Tagliabue, M., *see* Ferrari, R. 20 (1987) 91

Tellez-Giron, R., Ergang, K. and Hunger, A., A Combined Testing Approach for Instruction-Set-Based Data Processing Devices 20 (1987) 147
Ting, G.W., *see* Chao, Y. 20 (1987) 227
Tomas, S.P., *see* Shen, J.P. 20 (1987) 249
Trobec, R., Lesjak, I. and Subelj, M., A Resident X.25 Software Development 20 (1987) 55

Valenzano, A., *see* Ciminiera, L. 20 (1987) 59
Vasconcelos, N.Q., Franca, F.M.G. and Fernandes, E.S.T., Design of an Edison Virtual Machine – From a HLL Specification to a Microprogrammed Implementation 20 (1987) 209
Veler, Y., *see* Azaria, H. 20 (1987) 99
Vlajnic, M.S., WSI Implementation of Systolic Arrays for GaAs 20 (1987) 121

Yau, K.H., *see* Malek, K.H. 20 (1987) 331

Zoccolante, L., *see* Ferrari, R. 20 (1987) 91
Zulian, F. and Maccianti, T., Design of a VLSI 32-Bit Microprocessor to Be Used on the CPU (IDP) of the Honeywell DPS4 Follow-on Computer 20 (1987) 223